Further Thoughts from the 2017 SPIE AL EUV Lithography Conference

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Stochastics, Lent, Reporting on Conferences, Reality of Things, and a New SEMATECH

In the previous blog, I listed technology status and would now like to discuss a couple of topics in detail. During last year's SPIE AL conference, the message for EUVL was “Not If, but When.” This year the message was “Not If, but When and How Much Volume.” It was nice to see the technology that I bet on so long ago coming so far and doing so well.

Stochastics and LWR - Why This is not the End of EUVL and Optical Projection Lithography

The stochastics of photons and material were in the focus during the conference. One presenter even called it the cause of the “end of EUV and lithography.” Line width roughness (LWR), or the non-uniform and wiggly shapes of lines that form tiny electrical wires, affects the electrical properties of the circuits that we are working to produce in the end. Although these properties are better for circuits made with EUV compared to multiple patterning, EUV has a serious stochastics challenge as there are 14x fewer photons. I believe that that stochastics will be addressed in some ways and we must remind ourselves that our goal is not “patterns on resists,” which is an intermediate step, but to make “tiny patterns” in the material under the resist. We can beat the apparent limit of physics in how nicely we can transfer the image from mask to resist by finding solutions after the intermediate steps, as I elaborate on below.

First, LWR is not a new story. Back in the nineties, when 193 nm lithography was being developed, I was working in the ATDF fab at SEMATECH developing etch processes. I was told by many that LWR would kill 193 nm litho, as printed lines indeed looked terrible on resist, as well as when those images were transferred to the material below to form lines and contacts. I went to the library (yes, in those days you actually went to the library) trying to figure out the source of this problem, but did not get any clues. In the end

by trial and error, I found that a special post-resist patterning etch, initiated before the main etch, could clean up the pattern and drastically reduce LWR. I published a paper on it and did not think much of it at that time. This post-processing of resist patterns, now combined with post-litho rinses, new underlayers, new resist chemistries, litho- dep- etch optimization, flexible pupil illuminations, and innovative mask optical proximity correction (OPC) tricks, are among several knobs available to turn down LWR. Again, remember that resist image is only an intermediate step to what we are trying to do.

At this point, we need to remind ourselves that the Rayleigh criterion of resolution limits how small we can print using a given wavelength. However, we would not be printing what we can today if we had stopped at this resolution criterion. We have been overcoming this limit via OPC and other tricks, and the factor that quantifies our capability to print smaller is called k1. A whole industry emerged around how to take k1 as low as possible. When we approached the diffraction limit of 0.25 for k1 value, it was overcome by multiple patterning and the process continued. Eventually, to continue to print smaller and smaller in the quest toward atomic-level patterning, Litho needs to work together with deposition, etch and metrology. This is already happening, as demonstrated by several papers that showed joint development with etch suppliers.

I propose that the industry develop another factor like k1 (maybe call it s1) to measure how much we can reduce the effect of stochastics, with our goal being low s1 processes.

It is worthwhile to say a few things about Moore's Law and its projected end by many. I believe that Moore's Law in its true spirit is not only about physical scaling of the transistors, but also about the scaling of technology to allow ever-increasing information processing. I see transistors as "units of information processing." We will get to the limits of the current mode of scaling at atomic level patterning with circuit parameters that cannot be gainfully further improved, but that is not an end to scaling of the speed of information processing. In the end, we must switch to different technologies like quantum computing to continue the pace. However, I see no end in the next decade for the current form of scaling. Let us not forget that developing technology for scaling is not cheap, and not without lots of effort.

Lent

Ash Wednesday usually falls during the SPIE AL conference. Cathedral Basilica of St. Joseph is around the corner from the Fairmont in San Jose, where I usually stay. It has a beautiful interior and is worth a visit. I usually walk the blocks around the church until I get my required steps on Fitbit, and ponder on what I am going to give up this Lent – things that I very much enjoy and have not worked for me. This year, it

surprisingly appeared to me that the trade press was also observing Lent and had given up mockery and negative coverage on EUVL, which usually starts on Sunday after Nikon's Lithovision meeting, even before the start of the actual SPIE AL conference. It was unusually quiet this year on reporting.

Reporting on Conference News

Toward the end of the week, there were some press reports which contained some inaccuracy. During the conference, one keynote speaker complained to me that he was incorrectly quoted by the media. Another keynote speaker was widely quoted as saying something that was not said in the presentation.

I do not blame the press fully for this, as there is an inherent difficulty in news reporting of technical conferences. Those who are familiar with scriptures know this is a challenge that humanity has faced since ancient times –reporting on complicated things from a distance. The Bhagwat Gita starts with the inquiry of the blind king Dhritrashtra, who asks an expert, Sanjay, to report on what is happening in the far away battlefield (dhramshetra kurushete… kimkurvat Sanjaya – in the battlefield at Kurushetra, dear Sanjay, tell me what happened?). It's interesting to note that Sanjay himself was not at the battle and had to rely on other means to tell the story – such is the case for many of us who are basing their reports on what is being told by someone in the conference. I cannot blame the press too much, having myself missed on a couple of points now and then.

Reality of things – Lessons from Zen with Relevance to our Industry

As my Zen teacher says, "We like the idea of things but not the reality of things. Ordinary coping is an attempt to shape our experience to always match our idea of things. If our experience maps onto our precious idea of things, this is called 'happiness' or 'satisfaction'— getting what we want. This, we are taught, is the purpose of our lives and where we will find real meaning— it is the foundation for enjoying success." In Zen training we practice turning toward and engaging with the bare reality of things. He further adds, "We are not continually trying to shape ourselves or the world to fit our idea of things. We are meeting things just as they are and yet working with them as skillfully as we can. Zen practice encourages and supports this skillfulness."

When the industry got to immersion lithography, the biggest challenge was how to get rid of bubbles in the water. We certainly need to do a lot more and solve problems on many technical and infrastructure fronts. EUV indeed is complicated, as it not only involves a new type of scanner but also changing the infrastructure for mask, resist and modeling. Materials, high temperature plasmas, lasers, contamination, fabrication and

metrology— you name it. Moore's Law did not say that scaling is going to be easy or inexpensive– it just said that it will happen.

I may be the only person in the world who believes that "EUVL IS NOT LATE," and that "WE HAVE DONE WELL" with EUV technology development. Let us not forget how much time it took us to get immersion fully working, even though we had many fewer problems. The investment now is going to pay off. Chip makers know best, and so have decided on EUVL.

New SEMATECH

One last thing. During the conference I ran into Mark Melliar-Smith, ex-CEO of SEMATECH. it was a nice surprise, as I thought he had retired some time ago. I had just finished putting up an award on my office wall that I got from him many years ago. Seeing him reminded me of good old days of the semiconductor industry, when companies got together to address infrastructure challenges and consider technical challenges where success was not guaranteed. We saved money and tackled big challenges. It had to be done then, and later on we got away from the idea. It may be time to think about a new SEMATECH regarding efforts to extend Moore's Law. In my previous blog, I listed many things that a New SEMATECH (if we ever have it again) could do, like considering stochastics at the 5 and 7 sigma levels, new resist chemistries, and new types of sources such as those proposed by PSI. We will not get zero defect mask blanks without considering new materials, ultrafine polishing techniques and contamination control options. Chip makers (it is usually Intel which spends more than others) cannot do this alone, and suppliers cannot afford to look at these challenges on their own, either. If we want to pursue new frontiers to continue pushing Moore's Law forward, we need a new consortium like SEMATECH. I do not mind wishing for things, as that is the first step for things to happen! I leave you with a favorite quite from the Persian poet Hafez:

"I should not make any promises right now,
But I know if you
Pray
Somewhere in this world -
Something good will happen."

— Hafez